S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Xavier Vera et al.	Examiner:	Unknown
Serial No.:	Unknown	Group Art Unit:	Unknown
Filed:	Unknown	Docket:	P22414
Title:	CLUSTERED VARIATIONS-AWARE ARCHITECTURE		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the referenced materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Respectfully submitted,

XAVIER VERA ET AL.
By his Representatives,
Caven & Aghevli LLC

Date 12/22/05 By Ramin Aghevli

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	Unknown
Filing Date	December 22, 2005
First Named Inventor	Vera, Xavier
Art Unit	Unknown
Examiner Name	Unknown

Sheet	1	of	2	Attorney Docket No: P22414

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No**	**USP Document Number**	**Publication Date**	**Name of Patentee or Applicant of cited Document**	**Filing Date If Appropriate**

FOREIGN PATENT DOCUMENTS				
Examiner Initials*	**Foreign Document No**	**Publication Date**	**Name of Patentee or Applicant of cited Document**	**T[2]**

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		BORKAR, SHEKHAR, et al., "Parameter Variations and Impact on Circuits and Microarchitecture", DAC 2003, Copyright 2003 ACM 1-58113-688-9/06/0006,(June 2-6, 2003), 338-342	
		BROOKS, DAVID et al., "Dynamically Exploiting Narrow Width Operands to Improve Processor Power and Performance", Fifth International Symposium on High-Performance Computer Architecture (HPCA-5),, (January 1999), 10 pages	
		ERNST, DAN, et al., "Razor: A Low-Power Pipline Based on Circuit-Level Timing Speculation", Proceedings of the 36th International Symposium on Microarchitecture (MICRO-36'03), (2003), 12 pages	
		IYER, ANOOP, et al., "Power and Performance Evaluation of Globally Asynchronous Locally Synchronous Processors", International Conference on Computer Architecture Proceedings of the 29th annual international symposium on Computer architecture, (2002),158-168	
		MAGKLIS, GRIGORIOS, et al., "A FREQUENCY AND VOLTAGE SCALING ARCHITECTURE", Intel Ref #: P20449; Application Filed: November 29, 2004; Serial #: 10/999,786, 19 pgs.	
		MAGKLIS, GRIGORIOS, et al., "Frontend Frequency-Voltage Adaptation for Optimal Energy-Delay", 22nd IEEE International Conference on Computer Design: VLSI in Computers & Processors (ICCD 2004), San Jose, CA, USA, Proceedings. IEEE Computer Society 2004, (October 11-13, 2004), 250-255	

EXAMINER **DATE CONSIDERED**

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Examiner Name	Unknown

Sheet	2	of	2	Attorney Docket No: P22414

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		RESTLE, PHILLIP J., et al., "Timing Uncertainty Measurements on the Power5 Microprocessor", 2004 IEEE International Solid-State Circuits Conference, ISSCC 2004/ Session 19/ Clock Generation and Distribution/19.7, (2004),8 pages	
		SEMERARO, GREG, et al., "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling", Proceedings of the 8th International Symposium on High-Performance Computer Architecture, (2002), 12 pages	
		UNSAL, OSMAN, et al., "SYSTEM AND METHOD FOR EXPLOITING TIMING VARIABILITY", Intel Ref #:P21398; Application Filed: June 20, 2005, Serial #: 11/157,320., 31 pgs.	

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